Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A computer program product, tangibly embodied in an information carrier, for high speed queuing, the computer program product being operable to cause data processing apparatus to: ~~A computer instruction compromises:~~

execute a write queue descriptor count instruction that causes a processor to write a single word containing a queue count for each of a plurality of queue entries in a queue array cache.

2. (Currently amended) The computer program product ~~instructions~~ of claim 1 wherein the instruction includes: ~~further comprising:~~

an address field that specifies a location in memory of a queue descriptor.

3. (Currently amended) The computer program product ~~instructions~~ of claim 1 wherein the instruction includes: ~~further comprising:~~

an entry field that specifies a location of a queue descriptor in the queue array cache.

4. (Currently amended) A method comprising:

in a ~~processor~~ network device, maintaining a count field for queue descriptors of active output queues current in a memory of the network device.

5. (Presently amended) The method of claim 4 in which the count field is stored in a word, the word representing a unit of data of a defined bit length.

6. (Original) The method of claim 4 further comprising:

writing the count field subsequent to incrementing a count of buffers for a selected queue.

7. (Original) The method of claim 4 further comprising:

writing the count field subsequent to decrementing a count of buffers for a selected queue.

8. (Original) The method of claim 4 in which the count fields for queues descriptors are stored in a queue array cache.

9. (Original) Apparatus comprising:

a memory containing queue descriptors representing output queues, a queue manager programming engine and a content addressable memory (CAM);

a processor connected to the memory, the processor containing a memory controller, the memory controller having a cache containing a queue descriptor array for storing a subset of the queue descriptors; and

an array in memory for storing a count of queue descriptors in the subset.

10. (Original) The apparatus of claim 9 further comprising:

a plurality of microengines.

11. (Original) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

maintain a count field for queue descriptors of active output queues current in a memory.

12. (Currently amended) The computer program product of claim 11 in which the count field is stored in a word, the word representing a unit of data of a defined bit length.

13. (Original) The computer program product of claim 11 further comprising instructions to:

write the count field subsequent to incrementing a count of buffers for a selected queue.

14. (Original) The computer program product of claim 11 further comprising instructions to:

write the count field subsequent to decrementing a count of buffers for a selected queue.